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REMARKS

Rejection of Claims 49-56 and 59 Under 35 U.S.C. §102(b) based on *Chang* (U.S. Patent No. 4,958,321).

The invention of claim 49 is directed to a method for making a non-volatile semiconductor device. The method includes forming a multilayer gate dielectric having a charge storage layer. The multilayer gate dielectric is also dielectrically equivalent to a layer of silicon dioxide having a thickness that is less than 200 angstroms. The method further includes forming a gate comprising polycrystalline silicon of a first conductivity type on the gate dielectric. In addition, source and drain regions are formed that are separated by a channel region in a semiconductor substrate. The source and drain regions have a second conductivity type different than the first conductivity type.

The standard of anticipation, the ground under which these claims are rejected, is well established. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

Applicant has presented clear evidence that the reference *Chang* does not describe a gate of a first conductivity type in conjunction with source and drain regions of the second conductivity type.[1]

In rebutting Applicant's showing, the rejection relies on the following rationale:

> If a polysilicon gate is used instead of a metal gate, the polysilicon must be doped with a different conductivity type than the source/drain, that inversion and accumulation occur at different voltage.[2]

No citation is provided for this statement. Applicant has reviewed the reference relied upon, *Chang*, and submits that such a teaching is not included in the reference. In fact, *Chang* expressly teaches away from the present invention, by showing floating gate doping that is the

[1] See Applicant's Response to Office Action, dated July 19, 2002, Page 4, Line 21 to Page 5, Line 5.
[2] See the Office Action, dated 8/14/02, Page 2, Lines 11-13.

same type as source and drain doping.[3]

Because the above quoted statement is relied upon to establish anticipation, Applicant respectfully requests a citation for this statement, as it appears completely unsupported by the reference.

Further, Applicant submits the following additional evidence to refute the statement. Applicant's "Description of Related Art" describes at length how and why conventional MOSFETs and non-volatile memory transistors have like doping of gates and source/drain regions.[4]

Applicant's claim 49 includes additional elements not shown in the cited reference. *Chang* does not teach, expressly or inherently, a multilayer gate dielectric having a charge storage layer.

To show a multilayer gate dielectric with a charge storing layer the rejection relies on the following rationale:

> The inter-gate dielectric 116 (usually silicon oxide, or a combination of silicon oxide and nitride) and control gate 118, is formed on dielectric layer 110. This inter gate dielectric, which separates the floating gate from the control gate holds the bulk of charge that is injected into the floating gate.[5]

This statement, like that previous quotation, is made without citation. And, like the previous statement, Applicant has reviewed the reference relied upon and submits that such a teaching is not included in the reference.

Applicant strongly objects to this statement as it is entirely contrary to all teachings of *Chang*. *Chang* presents a conventional floating gate nonvolatile transistor. In such structures, charge is stored on the floating gate and not in a dielectric layer, as recited in claim 49.[6]

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[3] See *Chang*, Col. 7, Lines 7-9, which describes an actual doping for a floating gate being the density of donor dopants introduced. As is well known in the art, donor dopants produce an n-type doping. In support of this statement, see attached Exhibit A.

[4] See the Specification, Page 2, Lines 18-22, Page 2, Line 31 to Page 3, Line 3, and FIGS. 1-5, all of which show like doping between gate and source/drain regions (e.g., both n-type or both p-type).

[5] See the Office Action, dated 8/14/02, Page 2, Lines 13-16.

[6] See *Chang*, Col. 1, Lines 17-19, Col. 2, Lines 17-19 and Lines 52-54.

Applicant respectfully requests a citation for the above statement, as it also appears completely unsupported by the reference.

Because the rejection appears to rely on teachings outside of the cited reference to show all limitations of claim 49, and because such teachings contradict those of *Chang*, anticipation cannot have been established for this claim.

Claim 53, which depends from claim 49 adds the limitation of forming a charge storing layer selected from the group of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and a ferroelectric material.

To address the rejection of this claim, Applicant incorporates by reference herein the comments set forth above for claim 49. Namely, that in *Chang* a charge storing layer is doped polysilicon, which is a semiconductive material, and clearly different from the group of materials recited in claim 49.

For all of these reasons this ground for rejection is traversed.

Conditional Request for Reconsideration to Change Action from Final to Non-Final

The above rationales relied upon to reject claim 49 appear to present *modifications* of *Chang*. If this is the case, such rejections present a new ground of rejection, and hence the finality of the present office action is improper.

Accordingly, if the rejection is relying on a modification of *Chang*, Applicant respectfully requests reconsideration of the finality of this office action to establish a right of petition on this matter.

Rejection of Claims 57-59 Under 35 U.S.C. §103(a), based on *Chang* in view of *Vinal* (U.S. Patent 4,990,974).

Claims 57-59 depend from claim 49, and add various combinations of doping types and concentration.

As is well known, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

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To the extent that this ground for rejection relies on *Chang*, the comments set forth above for claim 49 are incorporated by reference herein. Namely, that various limitations of claim 49 are not shown in the reference.

It is not believed a prima facie case of obviousness has been established for claim 57, as motivation is lacking for the proposed combination of *Chang* in view of *Vinal*. As is well known it is improper to combine references where the references teach away from their combination.[7]

The reference *Vinal* teaches away from a combination with *Chang*.

The teachings of *Chang* are directed to "flash" EPROM cells.[8] According to *Chang*, programming flash EPROMs includes generating hot electrons for injection into a floating gate.[9] That is, generation of hot electrons is a necessary feature for the flash EPROMs of *Chang*.

Vinal is not related to any nonvolatile memory cell, let alone a flash EPROM, and remains directed to field effect transistor designs. *Vinal* is expressly directed at reducing hot electron generation – a feature necessary for the other reference *Chang*.[10]

Accordingly, because *Vinal* teaches away from combination with *Chang*, the necessary motivation for a prima facie case of obviousness is not believed to exist, and this ground of rejection is traversed.

Rejection of Claims 60-69 Under 35 U.S.C. §102(b) based on *Lancaster et al.* (U.S. Patent No. 4,958,321).

The invention of claim 60 includes a method with the steps of applying an electric field to a charge storing layer in a multilayer dielectric. The multilayer dielectric is disposed between a first semiconductor layer and a second semiconductor layer. The method also includes applying the electric field to form a charge accumulation region in the first semiconductor layer proximate to the multilayer gate dielectric and a charge depletion region in the second semiconductor layer proximate to the multilayer gate dielectric.

As previously noted, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

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[7] In re Grasselli, 218 USPQ 769, 779 (Fed. Cir. 1983).
[8] See *Chang*, the title, as well as Col. 5, Line 46, which describes every embodiment as a flash EPROM.
[9] See *Chang*, Col. 2, Lines 17-19.

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Applicant's claim 60 recites forming, by application of an electric field, a charge accumulation region proximate to multilayer gate dielectric **and** forming a charge depletion region proximate to the multilayer gate dielectric. That is, Applicant's method forms both an accumulation and depletion proximate to the gate dielectric.

To show such a limitation, the rejection relies on the following rationale:

> [W]hen a bias is applied to the gate of a device depending upon the polarity of the signal it either produces an accumulation of charges at the silicon/oxide interface or a depletion of charge at the silicon/oxide interface (emphasis added).[11]

As can be understood by the emphasized portions of the claim and rationale, regardless of whether the statement is correct or not, it cannot anticipate Applicant's claim 60. Applicant's claim 60 specifically recites forming both an accumulation region and a depletion region by application of an electric field. The above rationale only describes forming an accumulation region or a depletion region. Thus, all limitations have not been shown and hence anticipation has not been established.

For this reason, the rejection of claims 60-69 is traversed.

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[10] See *Vinal*, Col. 3, Lines 59-61, which describes the invention as a high speed MOS device with greatly reduced hot electron effects.

[11] See the Office Action, dated 8/14/02, Page 3, Lines 6-8.

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The present claims 49-69 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Bradley T. Sako
Reg. No. 37,923

Bradley T. Sako
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5315